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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,530	05/31/2001	Chia-Hsing Chen	148693.00367	1349

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EXAMINER
ROCCHEGIANI, RENZO

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/870,530	Applicant(s) CHEN, CHIA-HSING	
	Examiner Renzo N. Rocchegiani	Art Unit 2825	

-- Th MAILING DATE of this communication app ars on the cov r sh t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5, are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,933,733 (Feria et al.) in view of U.S. Patent No. 5,972,783 (Arai et al.)

Feria et al. disclose a process to form memory cells wherein a p-type semiconductor substrate is provided (col. 8, lines 15-25), whereon a dielectric layer is formed (Fig. 2). On the dielectric layer a photoresist layer is formed and patterned to expose a portion of the dielectric layer. (Fig. 3) An ion-implantation is performed to form pocket dopant regions (Fig. 5-6) and a second doping step is performed to form N-type ion-implanting regions in the p-type semiconductor substrate so as to form source and drain regions. (Fig. 4) Once the implantation steps have been performed the photoresist layers are removed. (Fig. 7).

Ferla et al. do not disclose the use of indium for the pocket implantation formation step.

Arai et al. teach a process for producing MOS transistor wherein a ion implantation step to form pocket regions comprises the implantation of indium. (col. 20, lines 15-20).

It would have been obvious to one having ordinary skill in the specific art to combine the teachings of Arai et al. to the invention disclosed by Ferla et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

3. Claims 2-4 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,933,733 (Ferla et al.) in view of U.S. Patent No. 5,972,783 (Arai et al.) and in further view of U.S. Patent N. 4,937,756 (Hsu et al.).

As stated in paragraph 2, all the limitations of the claims have been met except for teaching that the dielectric layer comprises ONO.

Ferla et al. disclose a dielectric layer comprises an oxide. (col. 4, lines 10-13).

Hsu et al. teach a process to form a gate structure wherein the gate insulation layer comprises an oxide that may be supplemented with deposited silicon nitride and oxynitride. (col. 3, lines 30-45).

It would have been obvious to one having ordinary skill in the specific art to combine the teachings of Hsu et al. to those of Eitan, since Hsu et al. teach that ONO structure would be the preferred material to be used thanks to its properties. (Hsu et al., col. 3, lines 48-55).

4. Claims 6, 9-11 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,933,733 (Feria et al.) in view of U.S. Patent No. 5,972,783 (Arai et al.) and in further view of U.S. Patent No. 6,030,871 (Eitan).

Feria et al. disclose a process to form memory cells wherein a p-type

semiconductor substrate is provided (col. 8, lines 15-25), whereon a dielectric layer is formed (Fig. 2). On the dielectric layer a photoresist layer is formed and patterned to expose a portion of the dielectric layer. (Fig. 3) The dielectric layer is then etched using the photoresist layer as a mask. (Fig. 3) An ion-implantation is performed to form pocket dopant regions (Fig. 5-6) and a second doping step is performed to form N-type ion-implanting regions in the p-type semiconductor substrate so as to form source and drain regions. (Fig. 4) Once the implantation steps have been performed the photoresist layers are removed. (Fig. 7).

Ferla et al. do not disclose the use of indium for the pocket implantation formation step. Ferla et al. also do not disclose the use of multi-layer photoresists.

Arai et al. teach a process for producing MOS transistor wherein a ion implantation step to form pocket regions comprises the implantation of indium. (col. 20, lines 15-20).

Eitan et al. teach the formation of memory cell with the implantation of pocket regions as well as source and drain regions wherein a plurality of photoresists layers are used. (Fig. 4C, 4E).

It would have been obvious to one having ordinary skill in the specific art to combine the teachings of Lin et al. to the invention disclosed by Ferla et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

It would have also been obvious to one having ordinary skill in the specific art to combine the teachings of Eitan to the invention disclosed by Ferla et al., since such process would provide an efficient way to form self-aligned pocket implants. (Eitan, col. 2, lines 1-8).

5. Claims 7-8, 12-13, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,933,733 (Ferla et al.) in view of U.S. Patent No. (Arai et al.) and of U.S. Patent No. 6,030,871 (Eitan) and in further view of U.S. Patent N. 4,937,756 (Hsu et al.).

As stated in paragraph 4, all the limitations of the claims have been met except for teaching that the dielectric layer comprises ONO.

Ferla et al. disclose a dielectric layer comprises an oxide. (col. 4, lines 10-13).

Hsu et al. teach a process to form a gate structure wherein the gate insulation layer comprises an oxide that may be supplemented with deposited silicon nitride and oxynitride. (col. 3, lines 30-45).

It would have been obvious to one having ordinary skill in the specific art to combine the teachings of Hsu et al. to those of Ferla et al., since Hsu et al. teach that ONO structure would be the preferred material to be used thanks to its properties. (Hsu et al., col. 3, lines 48-55).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renzo Rocchegiani whose telephone number is (703)

308-5839. The examiner can normally be reached on Monday through Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached at (703) 308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

RNR

May 31, 2002

D. Everhart
PRIMARY EXAMINER